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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Anatoliy V. Tsyrganovich	
Assignee:	ZiLOG, Inc.	
Title:	"Circle Correction in Digital Low-Pass Filter"	
Serial No.:	08/937,877	Filed: September 29, 1997
Patent No.:	7,139,037 B1	Issued: November 21, 2006
Examiner:	Vivek Srivastava	Group Art Unit: 2617
Doc. No.:	ZIL-183	

November 25, 2006

ATTN: Certificate of Correction Branch
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REQUEST FOR CERTIFICATE OF CORRECTION

Pursuant to 37 CFR 1.322, Applicant requests that the Director issue a certificate of correction to correct mistakes in the printing of the above-identified patent incurred through the fault of the Patent Office. Minor mistakes in the printing of claims 6 and 21 are clearly apparent when the attached pages of USP 7,139,037 B1 (marked to show the mistakes) is compared to the attached pages of the Listing of Claims that were submitted in the last amendment filed on May 10, 2006.

The word "a" should be added at the end of line 9 of claim 6, and a semicolon should replace a comma before the word "and" at the end of line 4 of claim 21.

Certificate

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of Correction

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Applicant: Anatoliy V. Tsyrganovich
Patent No.: 7,139,037 B1
Issue Date: September 29, 1997
Docket No.: ZIL-183

Text of the requested correction is submitted on the one attached page of Certificate of Correction form, PTO/SB/44.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: ATTN: Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

By Darien K. Wallace
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Date of Deposit: November 25, 2006

Respectfully submitted,

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PTO/SB/44 (04-05)
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,139,037 B1

APPLICATION NO.: 08/937,877

ISSUE DATE : November 21, 2006

INVENTOR(S) : Anatoliy V. Tsyrganovich

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6, line 16, the word "a" should be added to the end of the line after the word "provide".

Claim 6, lines 16-17 should read:

adding the adjustment signal to the input signal to provide a delayed output signal; and

Column 7, line 17, a semicolon should replace the comma before the word "and" at the end of the line.

Claim 21, lines 15-17 should read:

circuitry to constrain a phase signal within a finite preset range using a correction signal, wherein the correction signal is an integer multiple of 2π; and

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a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment signal being filtered, wherein the second circuit portion includes at least one coefficient circuit connected to one of the at least one delayed signal input and to the adjustment input, and wherein the output of the at least one coefficient circuit is to a second delay element and the output of the second delay element is sent to the at least one coefficient circuit.

2. A circuit comprising:

a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and

a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment signal being filtered, wherein the second circuit portion includes at least one coefficient circuit connected to one of the at least one delayed signal input and to the adjustment input, and wherein the coefficient circuit includes an input summer and a gain amplifier having a gain.

3. A circuit comprising:

a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and

a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of an output without the adjustment signal being filtered, wherein the first input and the output are phase representations, and wherein the adjustment input causes an integer multiple of 2π shift in the output signal.

4. A circuit comprising:

a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and

a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment being filtered; and

adjustment control logic adapted to provide the adjustment input, wherein the adjustment control logic is adapted to produce a minus 2π adjustment signal if a tested signal is greater than a positive reference value and produce a positive 2π adjustment signal if the tested signal is less than a negative reference value.

5. A circuit comprising:

a digital filter including input lines giving signal values at different time indexes, gain amplifier circuitry adapted to multiply the signal values by filter coefficients, and a summer connected to the gain amplifier circuitry to produce an output value; and

summing circuitry connected to the input lines of the signal values at different time indexes and to an adjustment input, wherein the output of the summing circuitry is sent to the gain amplifier circuitry.

6. A method comprising:

providing a circuit;

inputting an input signal into the circuit such that the circuit filters the input signal to provide a filtered component to the output of the circuit;

inputting an adjustment signal into the circuit so that the adjustment signal provides an unfiltered offset that is added to the output;

adding the adjustment signal to the input signal to provide a delayed output signal; and

adding the delayed output signal to the adjustment signal and the input signal.

7. The method of claim **6**, wherein the adjustment signal keeps the output within a preset range.

8. The method of claim **6**, wherein the filtering of the input signal is a low-pass filtering.

9. The method of claim **6**, wherein the input is a phase signal.

10. The method of claim **6**, wherein the input is a hue signal.

11. A method comprising:

constraining a phase signal within a finite preset range, the constraining step including adding a correction signal to the phase signal to produce an output;

adding a delay to the output;

feeding back the delayed output so that it is added to the correction signal and the phase signal; and

filtering the phase signal without filtering the correction signal portion of the phase signal.

12. The method of claim **11**, wherein the filtering of the modified phase signal is a low-pass filtering.

13. The method of claim **11**, wherein the constraining step is such that the phase signal is processed so as to use a differential input.

14. The method of claim **11**, wherein the phase signal is a hue signal.

15. A method comprising:

constraining a phase signal within a preset range, the constraining step including adding a correction signal to the phase signal; and

filtering the phase signal without filtering the correction signal portion of the phase signal, wherein the correction signal is an integer multiple of 2π.

16. A method comprising:

constraining a phase signal within a preset range, the constraining step including adding a correction signal to the phase signal; and

filtering the phase signal without filtering the correction signal portion of the phase signal, wherein the preset range is zero to 2π.

17. A method comprising:

constraining a phase signal within a preset range, the constraining step including adding a correction signal to the phase signal; and

filtering the phase signal without filtering the correction signal portion of the phase signal, wherein the preset range is zero to 2π plus a guard band.

18. The method of claim **17**, wherein the guard band is a reference value above or below the range zero to 2π.

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19. The method of claim 18, wherein the guard bands are $-\pi$ to zero and 2π to 3π.

20. A method comprising:

constraining a phase signal within a preset range, the constraining step including adding a correction signal to the phase signal; and

filtering the phase signal without filtering the correction signal portion of the phase signal, wherein the constraining step is such that the phase signal is processed so as to use a differential input, and wherein the differential input is offset by an integer multiple of 2π so as to reduce the absolute value of the differential input.

21. An apparatus comprising:

circuitry to constrain a phase signal within a finite preset range using a correction signal, wherein the correction signal is an integer multiple of 2π; and

a filter adapted to filter the phase signal without filtering the correction signal contribution, and to add the correction signal to the phase signal.

22. An electronic circuit comprising:

a delay which receives an input signal and outputs a delayed input signal;

a first adder which outputs a first corrected signal by adding a correction signal to the input signal;

a second adder which outputs a second corrected signal by adding the correction signal to the delayed input signal; and

a third adder which outputs an output signal by adding the first corrected signal and the second corrected signal.

23. A circuit comprising:

a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and

a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment being filtered; and

adjustment control logic adapted to provide the adjustment input, wherein the adjustment control logic is adapted to produce a minus 2π adjustment signal if a tested signal is greater than a first reference value and produce a positive 2π adjustment signal if the tested signal is less than a second reference value.

24. A circuit comprising:

a first circuit portion connected to a first input, the first circuit portion including at least one delay element;

a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment being filtered; and

adjustment control logic adapted to provide the adjustment input, wherein the adjustment control logic is adapted to produce a positive 2π adjustment signal if a tested signal is greater than a first reference value and produce a minus 2π adjustment signal if the tested signal is less than a second reference value.

25. A method comprising:

providing a first circuit portion connected to a first input, the first circuit portion including at least one delay element;

providing a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment being filtered; and

providing an adjustment input to produce a minus 2π adjustment signal if a tested signal is greater than a first reference value and produce a positive 2π adjustment signal if the tested signal is less than a second reference value.

26. A method comprising:

providing a first circuit portion connected to a first input, the first circuit portion including at least one delay element;

providing a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment being filtered; and

providing an adjustment input to produce a positive 2π adjustment signal if a tested signal is greater than a first reference value and produce a minus 2π adjustment signal if the tested signal is less than a second reference value.

* * * * *

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through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment being filtered; and

adjustment control logic adapted to provide the adjustment input, wherein the adjustment control logic is adapted to produce a minus 2π adjustment signal if a tested signal is greater than a positive reference value and produce a positive 2π adjustment signal if the tested signal is less than a negative reference value.

11. (canceled)

12. (currently amended) A circuit comprising:

a digital filter including input lines giving signal values at different time indexes, gain amplifier circuitry adapted to multiply the signal values by filter coefficients, and a summer connected to the gain amplifier circuitry to produce an output value; and

summing circuitry connected to the input lines of the signal values at different time indexes and to an adjustment input, wherein the output of the summing circuitry ~~being~~is sent to the gain amplifier circuitry.

13. (currently amended) A method comprising:

providing a circuit;

inputting an input signal into the circuit such that the circuit filters the input signal to provide a filtered component to the output of the circuit;

inputting an adjustment signal into the circuit so that the adjustment signal provides an unfiltered offset that is added to the output; ~~and~~

adding the adjustment signal to the input signal to provide a~~n~~ delayed output signal; and

adding the delayed output signal to the adjustment signal and the input signal.

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27. (original) The method of claim 18, wherein the phase signal is a hue signal.

28. (currently amended) An apparatus comprising:

circuitry to constrain a phase signal within a finite preset range using a correction signal[[;]], wherein the correction signal is an integer multiple of 2π; and

a filter adapted to filter the phase signal without filtering the correction signal contribution, and to add the correction signal to the phase signal.

29-30. (canceled)

31. (previously presented) An electronic circuit comprising:

a delay which receives an input signal and outputs a delayed input signal;

a first adder which outputs a first corrected signal by adding a correction signal to the input signal;

a second adder which outputs a second corrected signal by adding the correction signal to the delayed input signal; and

a third adder which outputs an output signal by adding the first corrected signal and the second corrected signal.

32. (previously presented) A circuit comprising:

a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and

a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment being filtered; and

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